

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Makoto Yamamoto et al.

**Serial No. 10/805,822**

(Divisional of 10/014,949 filed October 26, 2001)

**Filed: March 22, 2004**

For: **Method of Fabricating Semiconductor Integrated Circuit**

**Art Unit: 2811**

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# OFFICE OF PETITIONS

**Examiner: Tom Thomas**

Attorney Docket No.: 44471/298721

**CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8**

I hereby certify that this correspondence is being transmitted to the the Office of Petitions Facsimile Number (571.273.0025), on August 8, 2005.

2005. Janie Wilkins  
Janie Wilkins

DATE: August 8, 2005

## SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

**Mail Stop Petition  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450**

Sir:

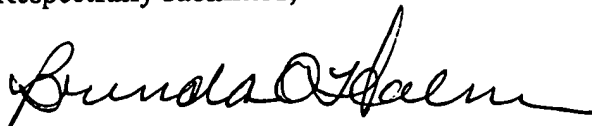
The citation of information on the attached Form PTO/SB/08A, "List of Art Cited by Applicant" is made pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98. A copy of each non-U.S. patent document listed is enclosed.

Each item of information contained in the attached Form PTO/SB/08A was first cited in the Office Action mailed on July 26, 2005 in a counterpart Japanese application. A copy of the Japanese Office Action (in Japanese) is also enclosed.

Second Supplemental Information Disclosure Statement  
Serial No. 10/805,822  
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The citation of this information does not constitute an admission of priority or that any cited item is available as a reference, or a waiver of any right Applicants may have under applicable statutes, Rules of Practice in patent cases, or otherwise. This Second Supplemental Information Disclosure Statement is being filed in connection with a Request for Continued Examination ("RCE"). Therefore, pursuant to 37 C.F.R. §§ 1.97(b)(4) Applicant believes that no fees are due beyond the fee for the RCE; however, the Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to Deposit Account No. 11-0855.

Respectfully submitted,



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